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# TRIPLE MODULAR REDUNDANCY LOW DELAY SINGLE ERROR CORRECTION CODE FOR PROTECTING DATA BITS

**T. VENKATESH & A. SRIDEVI**

Department of ECE, SNS College of Technology, Coimbatore, Tamil Nadu, India

## ABSTRACT

Error correction codes are used for long years to protect memories from the soft errors. For a single bit error correction, the SEC single bit error correction code that correct one bit error per word are used. Double bit error detection code are used to detect the double bit errors. In the increasing of the technology the single bit error correction codes are used in the various places such as it is used to protect the registers. Suppose if we use the error correcting code means it affects the area delay added by the circuit. In case of the memory these are more important such that these extra bits are getting added to the each code word. For that the newly proposed codes are targeting to reduce the number of bits added by the code. In this paper a method to construct the low delay single error correction code is proposed. In order to increase the reliability of the circuit the Triple Modular redundancy is used. If the output of the decoder is taken three times at the input of the triple modular redundancy if any stuck at fault occurs on the data bits means it can be able to overcome the error and it will produce the correct output. If there is an error occur during one of the Triple modular redundancy method means also it can be able to recover the output correctly.

**KEYWORDS:** Error Correction Code (ECC), Single Error Correction Codes (SEC), Soft Errors